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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,665	10/06/2003	George Matamis	SNDK.294US0	5425

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EXAMINER	
DOTY, HEATHER ANNE	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 12/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/680,665	MATAMIS ET AL.	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 8-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-5,8,9 and 22-26* is/are allowed.

6)☒ Claim(s) *10-16,18-20 and 27-31* is/are rejected.

7)☒ Claim(s) *17,21 and 32-34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/16/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 20 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 20 recites the limitation "the means within the substrate for isolating adjacent floating gates" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim. For the purposes of determining patentability, the examiner assumes that the means within the substrate for isolating adjacent floating gates is the means for isolating floating gates in the wordline direction.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless – (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 10-14 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Joo et al. (U.S. 6,204,122).

Regarding claim 10, Joo et al. teaches a non-volatile memory device comprising floating gates that store a charge (50 in Fig. 7B); bitlines that select amongst the floating gates, each bitline having a bitline axis (Fig. 2B shows general bitline direction layout; Fig. 7B shows invention in bitline direction; column 5, lines 60-64); wordlines that select amongst the floating gates (**58** in Figs. 7A and 7B; column 6, lines 6-11); and

conductive sidewall elements positioned along the bitline axes, the sidewall elements located at sides of the floating gates between adjacent floating gates, the sidewall elements shielding the floating gates (**46** in Fig. 9B; column 7, lines 15-18; since the sidewall elements are conductive, they shield the floating gates).

Regarding claim 11, Joo et al. teaches the memory device of claim 10, wherein the sidewall elements shield the floating gates from an electrical field having a component in the direction of the bitline axes (Fig. 7B shows conductive spacers oriented perpendicular to the bitline direction, which shield the floating gates in the bitline direction).

Regarding claim 12, Joo et al. teaches the memory device of claim 10, wherein the sidewall elements extend from the substrate to the floating gates (Fig. 9B).

Regarding claim 13, Joo et al. teaches the memory device of claim 12, wherein the floating gates have an uppermost and a lowermost surface, the sidewall elements extending from the substrate until or beyond the level of the lowermost surface (Fig. 9B).

Regarding claim 14, Joo et al. teaches the memory device of claim 12, wherein the floating gates have an uppermost and a lowermost surface, the sidewall elements extending from the substrate until or beyond the level of the uppermost surface (Fig. 9B).

Regarding claim 18, Joo et al. teaches a method of forming flash memory comprising forming floating gates (42 in Fig. 9B); forming control gates above the floating gates (58 in Fig. 7B); forming bitlines, the bitlines used together with the control

gates to read and write from a floating gate (Fig. 2B shows general bitline direction layout; Fig. 7B shows invention in bitline direction; column 5, lines 60-64), the direction of the bitlines substantially perpendicular to the direction of the control gates, the floating gates having bitline sides in the bitline direction (Fig. 7B) and control gate sides in the control gate direction (Fig. 7A); and forming conductive members (**46** in Fig. 9B) between the bitline sides of the floating gates, the members shielding the floating gates from electrical fields having a component in the bitline direction (Fig. 7B—since the members are conductive and are located between floating gates in the bitline direction, they shield the floating gates from electrical fields having a component in the bitline direction). The phrase "NAND flash memory" has not been given patentable weight, since it is recited only in the claim preamble, and none of the claimed method steps limit the device to a NAND flash memory.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless – (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 10-16, 18, 19 and 27-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Van Duuren et al. (U.S. 2005/0218445).

Regarding claim 10, Van Duuren et al. teaches a non-volatile memory device comprising floating gates that store a charge (**14** in Fig. 10); bitlines that select amongst the floating gates, each bitline having a bitline axis (Figs. 1 and 3-10 show the invention

in the bitline direction—in contrast, Fig. 2 shows the perpendicular wordline direction, paragraph 0041; Van Duuren et al. does not expressly teach forming the bitline, but it is an inherent feature of the memory device); and conductive sidewall elements positioned along the bitline axes, the sidewall elements located at sides of the floating gates between adjacent floating gates, the sidewall elements shielding the floating gates (**24** in Fig. 10).

Regarding claim 11, Van Duuren et al. teaches the memory device of claim 10, wherein the sidewall elements shield the floating gates from an electrical field having a component in the direction of the bitline axis (Fig. 10—since the sidewall elements are conductive and located between floating gates in the bitline direction, they will shield the floating gates from an electrical field having a component in the direction of the bitline axis).

Regarding claim 12, Van Duuren et al. teaches the memory device of claim 10, wherein the sidewall elements extend from the substrate to the floating gates (Fig. 10).

Regarding claims 13 and 14, Van Duuren et al. teaches the memory device of claim 12, wherein the floating gates have an uppermost and a lowermost surface, the sidewall elements extending from the substrate until or beyond the level of the lowermost surface and the uppermost surface (Fig. 10).

Regarding claim 15, Van Duuren et al. teaches the memory device of claim 10, wherein the sidewall elements comprise a conductive material and wherein the sidewall elements are electrically coupled to a wordline located between adjacent pairs of sidewall elements (Fig. 9; paragraph 0061—wordline is the control gate **18** in Fig. 2).

Regarding claim 16, Van Duuren et al. teaches the memory device of claim 15, wherein the coupled sidewalls effectively increase the surface area of the wordline and the electrical coupling between the wordline and the floating gates, thereby aiding in read and write operations (paragraph 0061—since the coupled sidewalls are electrically connected to the wordline, they must effectively increase the surface area of the wordline, which inherently aids in read and write operations, as disclosed in the instant specification in paragraph 0028).

Regarding claim 18, Van Duuren et al. teaches a method for forming flash memory comprising forming floating gates (**14** in Fig. 10); forming control gates above the floating gates (18 in Fig. 10); forming bitlines, the bitlines used together with the control gates to read and write from a floating gate, the direction of the bitlines substantially perpendicular to the direction of the control gates, the floating gates having bitline sides in the bitline direction and control gate sides in the control gate direction (Figs. 1 and 3-10 show the invention in the bitline direction—in contrast, Fig. 2 shows the perpendicular wordline direction, paragraph 0041; Van Duuren et al. does not expressly teach forming the bitline, but it is an inherent feature of the memory device); and forming conductive members between the bitline sides of the floating gates, the members shielding the floating gates from electrical fields having a component in the bitline direction (**24** in Fig. 10—since the sidewall elements are conductive and located between floating gates in the bitline direction, they will shield the floating gates from an electrical field having a component in the direction of the bitline axis).

Regarding claim 19, Van Duuren et al. teaches a flash memory device comprising floating gates for storing data located above a substrate (**14** in Fig. 10); means for isolating adjacent floating gates in the wordline direction (**11** in Fig. 2; paragraph 0041); means for isolating adjacent floating gates in the bitline direction (conductive spacers **24** in Fig. 10); and means for reading the data stored in the floating gates, the means for reading the data located above the floating gates and interconnecting strings of floating gates, the means for isolating adjacent floating gates in the bitline direction electrically connected to the means for reading the data (control gates 18 in Figs. 2 and 10; paragraph 0061 describes how the control gates are electrically connected to the conductive spacers).

Regarding claim 27, Van Duuren et al. teaches a method of making a non-volatile memory array, comprising a plurality of floating gates (**14** in Fig. 10) and forming a plurality of control gates (**18** in Fig. 10; paragraph 0039 specifies that the elements are plural) extending in a first direction and overlying the plurality of floating gates; forming insulating elements along sides of the plurality of floating gates that extend in the first direction (**22** in Fig. 5; paragraph 0051), the insulating elements extending above lower surfaces of the plurality of control gates (Fig. 5); and forming conductive sidewall portions overlying insulating elements (**24** in Fig. 10), the conductive portions in contact with control gates, but insulated from floating gates by the insulating elements (Fig. 9; paragraph 0061).

Regarding claim 28, Van Duuren et al. teaches the method of claim 27, wherein the insulating elements are first formed to extend along the sides of the plurality of the

floating gates and along sides of the plurality of control gates and are subsequently etched to provide a contact area to the control gates (paragraph 0050).

Regarding claim 29, Van Duuren et al. teaches the method of claim 27, further comprising, subsequent to the forming the conductive sidewall portions, implanting source and drain regions (**20** in Fig. 8; paragraph 0048).

Regarding claim 30, Van Duuren et al. teaches the method of claim 29, further comprising forming protective spacers on sides of the conductive sidewall portions (**32** in Fig. 8), and wherein the implanting is in a region defined by the protective spacers (Fig. 8 shows the boundary of implant region **20** corresponding to the boundary of spacer **32**).

Regarding claim 31, Van Duuren et al. teaches a plurality of floating gates on a substrate (**14** in Fig. 10); a plurality of control gates, an individual control gate overlying a floating gate of the plurality of floating gates so that first and second sides of the control gate are coplanar with first and second sides of the floating gate (**18** in Fig. 10; paragraph 0039 specifies that the elements are plural); a first insulating element covering the first side of the floating gate and extending to partially cover the first side of the control gate (unlabelled in Fig. 10 on left side of floating and control gates); a second insulating element covering the second side of the floating gate and extending to partially cover the first side of the control gate (unlabelled in Fig. 10 on right side of floating and control gates); a first conductive sidewall that extends from the first side of the control gate and overlies the first insulating element (**24** on left side of Fig. 10); and

a second conductive sidewall that extends from the second side of the control gate and overlies the second insulating element (**24** on right side of Fig. 10).

Allowable Subject Matter

Claim 20 would be objected to as being dependent upon a rejected base claim if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Claims 17, 21 and 32-34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 17, Van Duuren et al. does not teach that the non-volatile storage device is a NAND flash memory.

Regarding claims 20 and 21, prior art does not teach or suggest, in combination with the other claimed limitations, that the means for reading the floating gates extends within means within the substrate for isolating adjacent floating gates.

Regarding claims 32-34, prior art does not teach or suggest, in combination with the other claimed limitations, a T-shaped floating gate. Van Duuren et al. does not teach floating gates with T-shaped cross sections, and there is no motivation to combine this reference with other relevant prior art.

Claims 1-5, 8, 9, and 22-26 allowed for reasons given in the Office action dated 6/20/2005.

Response to Arguments

Applicant's arguments with respect to claims 10-16, 18, and 19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

had

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